## REMARKS

Claims 1 - 6, 8 and 10 - 13 are pending in the present application. By this Amendment, claims 7, 9, 14, 15 and 16 have been canceled without prejudice or disclaimer and and claims 4, 5, and 8 have been amended. Applicants respectfully submit that no new matter has been added. Applicants believe that this Amendment is fully responsive to the Office Action dated **July 5, 2002**.

ALLOWABLE SUBJECT MATTER:

Applicants gratefully acknowledge the indication in the Office Action that claims 10 - 13 are allowed and that claims 4 and 5 would be allowable, if amended, in independent form to include the features of their respective base and intervening claims.

In view of the above, claims 4 and 5 have been amended in independent form to include all of the limitations of their respective base and intervening claims. Therefore, it is respectfully submitted that claims 4 - 5 are now allowable.

AS TO THE MERITS:

As to the merits of this case, the Examiner sets forth the following rejections:

1) claims 1 - 3, 7, 8 and 9 stand rejected under 35 U.S.C. §102(b) as being anticipated by Ushiku, et al. (U.S. Patent No. 5,032,890).

2) claims 1 and 6 stand rejected under 35 U.S.C. §102(b) as being anticipated by Bothra, et al. (U.S. Patent No. 6,020,616); and

3) claims 7 and 9 stand rejected under 35 U.S.C. §103(e) as being anticipated by Shin (U.S. Patent No. 6,384,464).

All of these rejections are respectfully traversed.

**Claims 1-3 and 6:**

Ushiku is directed to addressing difficulties in forming a pattern on the insulating film 60 that is not flat at positions where no interconnection layer pattern is provided (Fig. 4B). In Fig.7, dummy patterns 20, 30a-30c, and 40 are provided where patterns 22, 32, and 42 are not located, thereby making it possible to form a flat insulating film on top of these patterns. On this insulating film, patterns 201 and 205 are provided as upper-layer patterns.

In Ushiku as described above, the dummy patterns and the patterns 22, 32, and 42 are provided in the same layer, with the upper-layer patterns 202 and 204 being formed on the dummy patterns.

Accordingly, Ushiku does not teach providing dummies in a layer different from a layer in which wires are provided such that the dummies are arranged to avoid areas overlapping the position of these wires.

Bothra shows, in Fig. 3L, active regions (transistors) 204, dummy active regions 214, polysilicon gates 216, and dummy polysilicon lines 226. The examiner asserts that the dummy polysilicon lines 226 are formed in non-overlapping relationship to active regions 204 of the substrate and in non-overlapping relationship to the active wiring network (polysilicon gates 216). As shown in Fig.2B, the dummy polysilicon lines 226 and the polysilicon gates 216 are formed in the same layer.

Accordingly, Bothra does not teach providing dummies in a layer different from a layer in which wires are provided such that the dummies are arranged to avoid areas overlapping the position of these wires.

**Claim 8:**

Neither Ushiku nor Shin teaches dummy patterns having different sizes and arranged at respective different pattern intervals.

In view of the aforementioned amendments and accompanying remarks, claims 1 - 6, 8 and 10 - 13 are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with markings to show changes made

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## VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/994,753

**IN THE CLAIMS:**

Claims 7, 9, 14, 15 and 16 have been CANCELED without prejudice or disclaimer.

Claims 4, 5, and 8 have been AMENDED to read as follows:

4. (AMENDED) A semiconductor integrated circuit [as claimed in claim 3], comprising:

a plurality of layers provided on a semiconductor substrate;

wires provided in a first layer that is one of said plurality of layers; and

wire dummies provided in a second layer different from the first layer and having an arrangement that avoids areas overlapping positions of said wires,

wherein said wires are signal wires excluding power supply wires, and

said wire dummies are further provided in areas overlapping positions of said power supply wires that are provided in the first layer.

5. (AMENDED) A semiconductor integrated circuit [as claimed in claim 4], comprising:

a plurality of layers provided on a semiconductor substrate;

wires provided in a first layer that is one of said plurality of layers; and

wire dummies provided in a second layer different from the first layer and having an arrangement that avoids areas overlapping positions of said wires,

wherein said wires are signal wires excluding power supply wires,

said wire dummies are further provided in areas overlapping positions of said power supply wires that are provided in the first layer, and

said signal wires have a width less than a predetermined wire width, and said power supply wires have a width greater than the predetermined wire width.

8. (AMENDED) A semiconductor integrated circuit [as claimed in claim 7], comprising:

a wire layer;

wires provided in said wire layer; and

dummy patterns provided in said wire layer and having different sizes,

wherein said dummy patterns having different sizes are arranged at respective different pattern intervals.